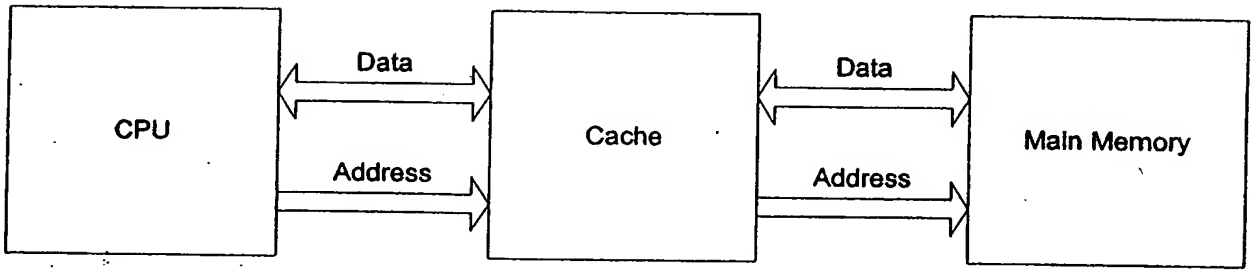


Figure 1.

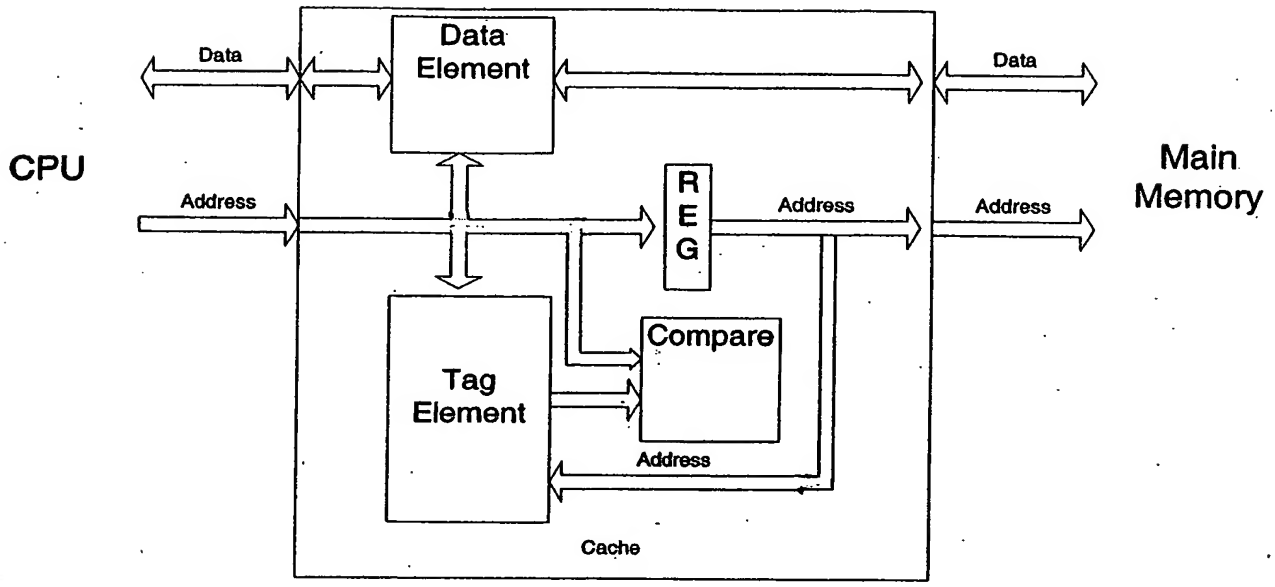

CPU
Data
Address
Data Element
R
E
G
Tag Element
Compare
Address
Cache
Data
Address
Address
Main Memory

Figure 2.

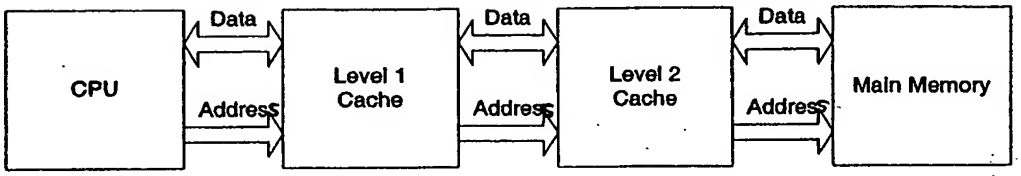

CPU
Data
Address
Level 1 Cache
Data
Address
Level 2 Cache
Data
Address
Main Memory

Figure 3.

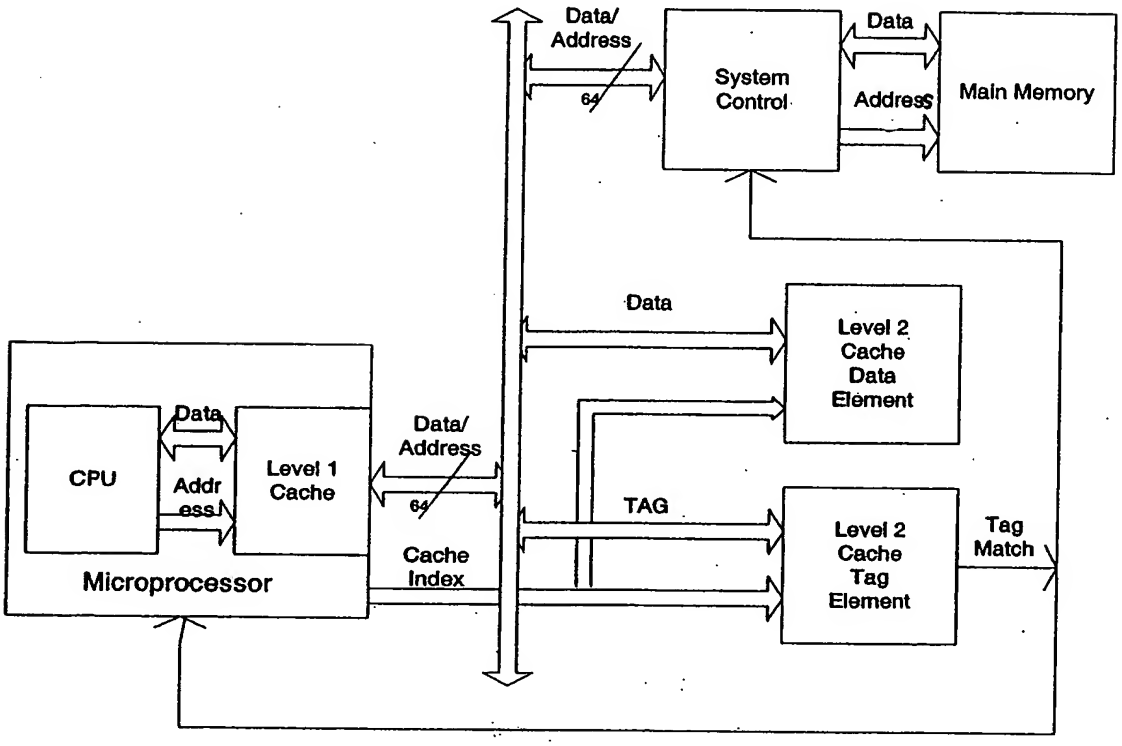

Data/
Address
64
System
Control
Data
Address
Main Memory
Data
Level 2
Cache
Data
Element
CPU
Data
Addr
ess
Level 1
Cache
Data/
Address
64
TAG
Level 2
Cache
Tag
Element
Tag
Match
Cache
Index
Microprocessor

Figure 4.

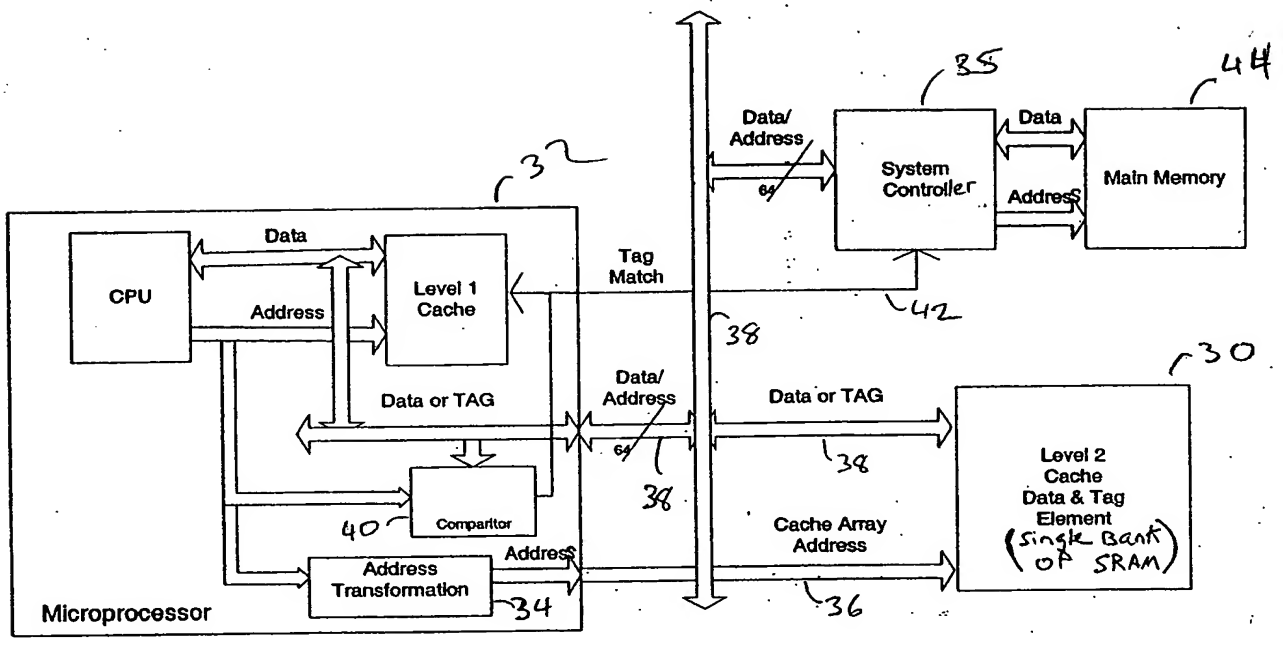

32
CPU
Data
Address
Level 1 Cache
Data or TAG
Comparitor
40
Address Transformation
34
Address
Microprocessor
Tag Match
38
Data/ Address
64
38
Data or TAG
38
Cache Array Address
36
Level 2 Cache Data & Tag Element (single Bank of SRAM)
30
Data/ Address
64
System Controller
35
42
Data
Address
Main Memory
44

Figure 5.

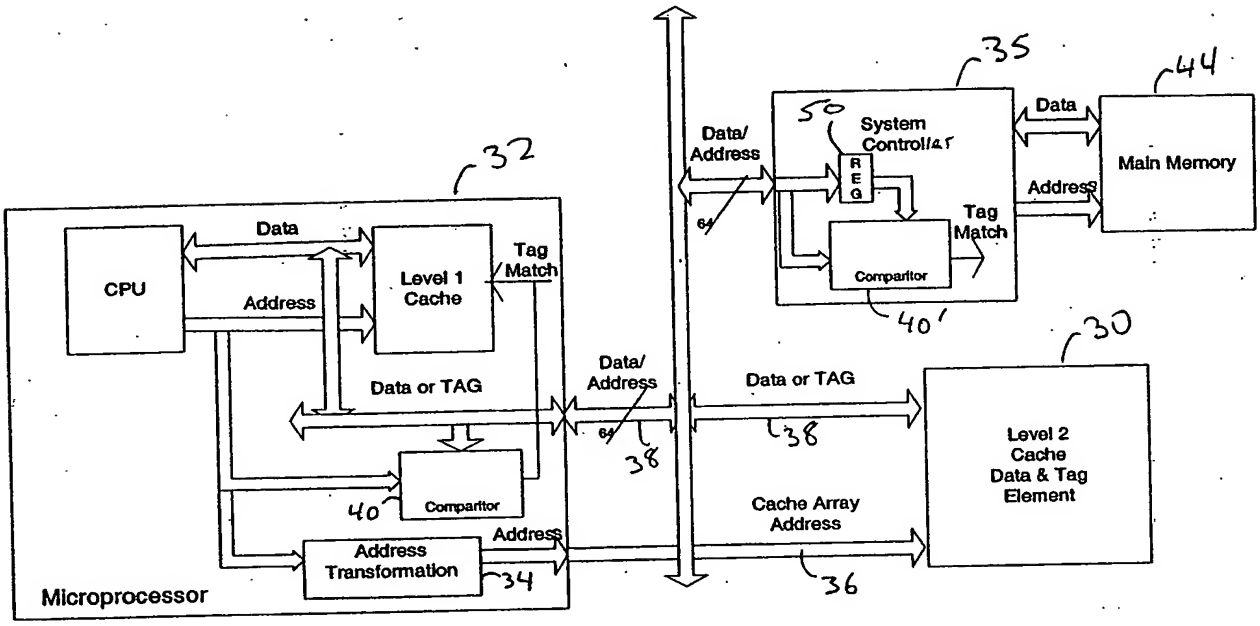

32
CPU
Data
Address
Level 1 Cache
Tag Match
Data or TAG
Comparitor
40
Address Transformation
Address
34
Microprocessor
Data/ Address
64
38
35
50
System Controller
REG
Tag Match
Comparitor
40'
Data
Address
Main Memory
44
Data or TAG
38
30
Level 2 Cache Data & Tag Element
Cache Array Address
36

Figure 6.

Fig. 7

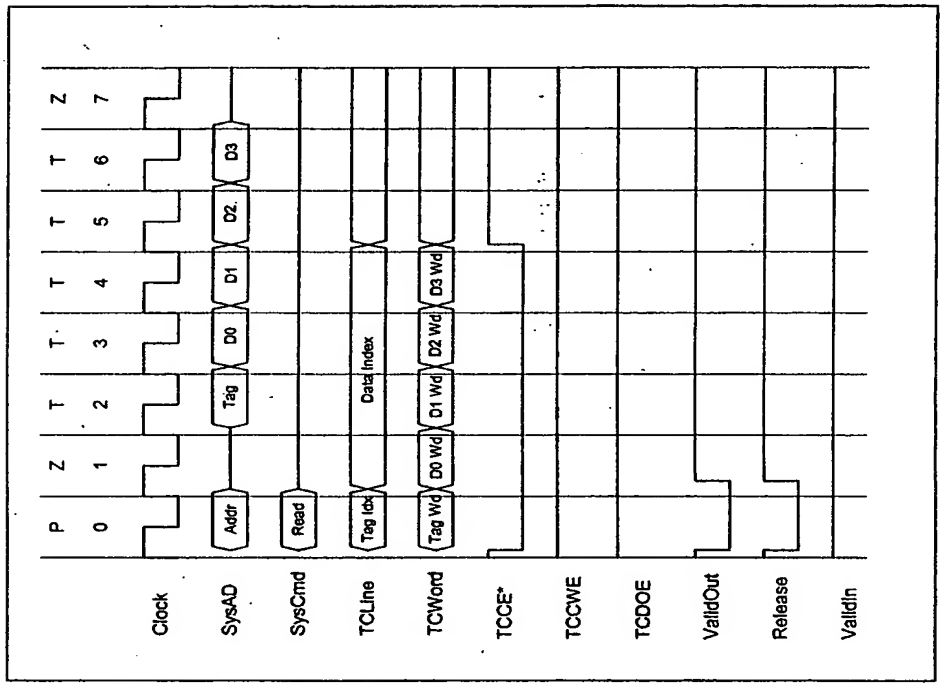
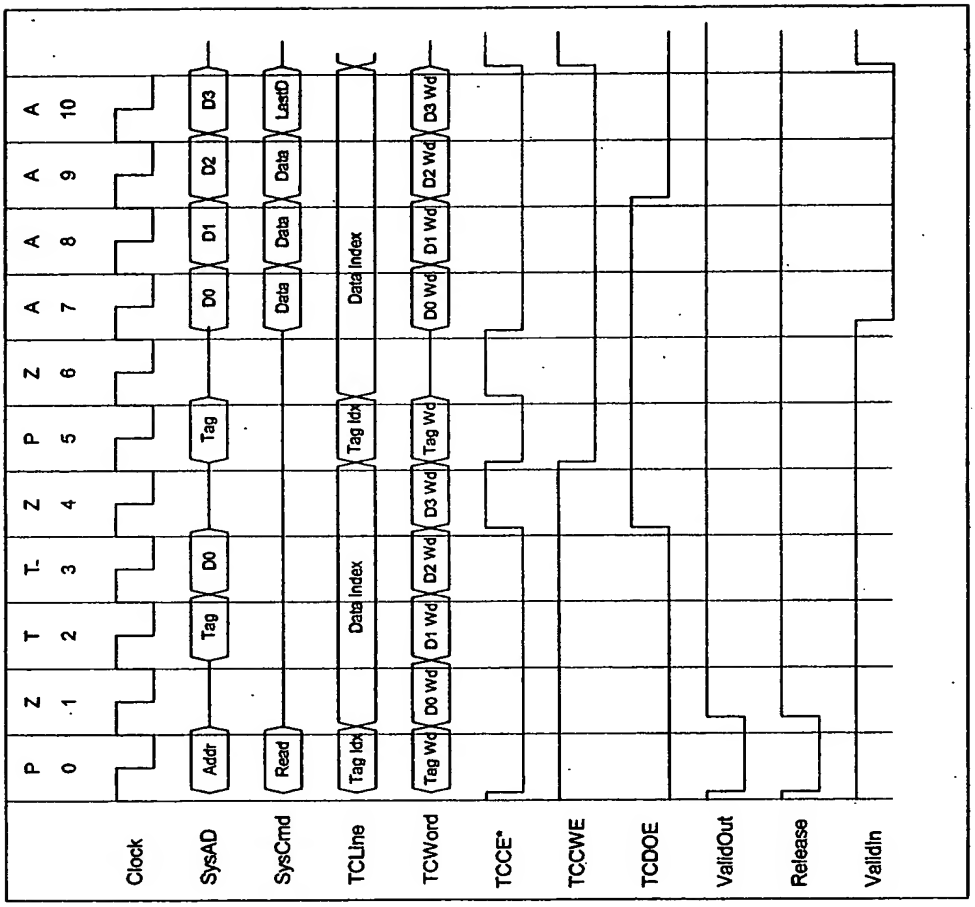

P
0
Z
1
T
2
T
3
T
4
T
5
T
6
Z
7
Clock
SysAD
Addr
Tag
D0
D1
D2
D3
SysCmd
Read
TCLine
Tag Idx
Data Index
TCWord
Tag Wd
D0 Wd
D1 Wd
D2 Wd
D3 Wd
TCCE*
TCCWE
TCDOE
ValidOut
Release
ValidIn

Fig. 8


P 0
Z 1
T 2
T 3
Z 4
P 5
Z 6
A 7
A 8
A 9
A 10
Clock
SysAD
SysCmd
TCLine
TCWord
TCCE*
TCCWE
TCDOE
ValidOut
Release
ValidIn
Addr
Tag
D0
D1
D2
D3
Read
Data
LastD
Tag Idx
Data Index
Tag Wd
D0 Wd
D1 Wd
D2 Wd
D3 Wd